

QUERY CONTROL FORM		RTIS USE ONLY	
Application No.	09/541,460	Prepared by	NRB
Examiner-GAU	Phan-2818	Date	3/10/04
		No. of queries	1FW
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## JACKET

- |                      |                        |                    |                |
|----------------------|------------------------|--------------------|----------------|
| a. Serial No.        | f. Foreign Priority    | k. Print Claim(s)  | p. PTO-1449    |
| b. Applicant(s)      | g. Disclaimer          | l. Print Fig.      | q. PTOL-85b    |
| c. Continuing Data   | h. Microfiche Appendix | m. Searched Column | r. Abstract    |
| d. PCT               | i. Title               | n. PTO-270/328     | s. Sheets/Figs |
| e. Domestic Priority | j. Claims Allowed      | o. PTO-892         | t. Other       |

## SPECIFICATION

- Page Missing
- Text Continuity
- Holes through Data
- Other Missing Text
- Illegible Text
- Duplicate Text
- Brief Description
- Sequence Listing
- Appendix
- Amendments
- Other

## CLAIMS

- a. Claim(s) Missing
- b. Improper Dependency
- c. Duplicate Numbers
- d. Incorrect Numbering
- e. Index Disagrees
- f. Punctuation
- g. Amendments
- h. Bracketing
- i. Missing Text
- j. Duplicate Text
- k. Other

## MESSAGE

Claim 5 (originally claim 6) ends with a semicolon — incomplete.

Please advise/provide missing data.

Thank you

initials *QMP*.

## RESPONSE

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(Previously amended) In combination:

an analog to digital converter having an input terminal and an output terminal;

a programmed gain preamplifier having an input terminal for receiving an input signal, an offset terminal, and an output terminal;

a digital summing junction;

said output terminal of said analog to digital converter coupled to said digital summing junction;

an anti-alias filter having an input terminal and an output terminal;

said output terminal of said anti-alias filter coupled to said input of said analog to digital converter;

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said input terminal of said anti-alias filter coupled to said output terminal of said programmed gain preamplifier; and,

said digital to analog converter coupled between said digital summing junction and said offset terminal of said programmed gain preamplifier for providing an analog offset signal to said programmed gain preamplifier.

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(Previously amended) The combination:

an analog to digital converter having an input terminal and an output terminal;

a programmed gain preamplifier having an input terminal for receiving an input signal, an offset terminal, and an output terminal;

a digital summing junction;

said output terminal of said analog to digital converter coupled to said digital summing junction;

an anti-alias filter having an input terminal and an output terminal/.

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said output terminal of said anti-alias filter coupled to said input of said analog to digital converter;

said input terminal of said anti-alias filter coupled to said output terminal of said programmed gain preamplifier;

said digital to analog converter coupled between said digital summing junction and said offset terminal of said programmed gain preamplifier for providing an analog offset signal to said programmed gain preamplifier; and,

wherein said programmed gain preamplifier provides a high differential gain for said input signal and a low single-ended gain for said analog offset signal;

7. (Canceled) In the method of operating an analog to digital converter for resolution enhancement, the steps of:

displacing the input signal range of the analog to digital converter to one of a plurality of overlapping positions comprising offset bands wherein the width of each band is representative of the input signal range of the analog to digital converter; and,

overlapping the offset positions to provide hysteresis.

8. (Canceled) A method for resolution enhancement in an analog to digital converter comprising the steps of:

converting a reference voltage of more than a least significant bit;

subtracting a mathematically-derived reference voltage of more than a least significant bit from the circuit's input voltage; and then

adding the converted reference voltage of more than a least significant bit to the converted reduced input voltage.